REMARKS

Some of the rejected claims have been amended. No new matter has been added.

Applicants submit this Amendment "C" and response with the accompanying CPA for the Examiner's consideration. Reexamination and reconsideration of the application, as amended, in view of the following remarks are respectfully requested.

1. STATUS OF THE CLAIMS

Claims 1-43 were presented for examination; claims 1-43 stand rejected and pending in the application. The rejections are addressed hereinbelow.

2. RESPONSE TO REJECTIONS

2.1. *Claim Rejections Under 35 U.S.C. § 112 ¶ 1*

Claims 35-41 stand rejected under 35 U.S.C. § 112 ¶ 1. The recitation that the spacer and the isolation trench are formed with a single etch recipe has been deleted in the pending claims, and thus this rejection is presently moot. This deletion has been introduced for advancing the case in the examination process and without prejudice of introducing claims with such language and/or traversing the rejection grounds at a later stage or in a continuation application.

2.2. *Claim Rejections Under 35 U.S.C. § 102(b)*

Claims 1, 6-8, 11, 41, and 43 stand rejected in light of Omid-Zohoor, U.S. Pat. No. 6,097,072 (hereinafter "the '072 patent "). These claims presently recite at least one of the following features: forming at least one isolation trench that has a rounded top edge; planarization that is performed in the absence of masking of the conformal layer over at least one isolation trench; and planarization

with a single etch recipe (and language variations thereof). In contrast, none of these features is disclosed in the '072 patent.

Claim 38 stands rejected under 35 U.S.C. § 102(e) in light of the '072 patent. This rejection is respectfully traversed because claim 38 recites two material layers within each isolation trench. In contrast, the '072 patent discloses only one oxide layer 372 filling each isolation trench described therein.

Because of at least the foregoing recited features, the '072 patent, does not disclose each and every step of the methods recited in these claims. Consequently, the '072 patent does not anticipate the methods recited in these claims. Applicants respectfully submit that claims 1, 6-8, 11, 38, 41, and 43 patentably distinguish over the '072 patent, and reconsideration and withdrawal of this rejection is respectfully requested.

2.3. *Claim Rejections Under 35 U.S.C. § 103(a)*

Claims 9-10, 12-13, 18-37, 39-40 and 42 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Lee, U.S. Pat. No. 5,229,316 (hereinafter "Lee"), with at least another reference.

The present patent application is a continuation of U.S. Pat. Application Serial No. 08/985,588, filed 12/05/97, now U.S. Pat. No. 5,953,621, which is a divisional of U.S. Pat. Application Serial No. 08/823,609, filed 03/25/97. A copy of the assignment document of this parent application, recorded at the U.S. Patent and Trademark Office at reel/frame 8488/0262, is attached hereto showing assignment by the inventive entity to Micron Technology, Inc., which is listed as the assignee of Lee.

Given the effective filing date of the present application, Lee is disqualified under 35 U.S.C. § 103(c) from being prior art against the presently claimed invention because the subject matter

disclosed in Lee and the presently claimed invention were, at the time the invention was made, commonly owned, or subject to an obligation of assignment to the same person.

For the foregoing reasons, Applicants respectfully request reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) that rely on Lee as a reference.

Independent claim 14 and its dependent claims 15-17 stand rejected under 35 U.S.C. § 103(a) as obvious over the '072 patent in combination with Poon *et al.*, U.S. Pat. No. 5,387,540 (hereinafter "Poon"). In addition to the reasoning provided in Amendment "B" and response regarding this combination of references, Applicants note that claims 14-17 recite, directly or by incorporation, distinguishing features such as the formation of isolation trenches with rounded top edges. This is not a mere geometrical variation taught by the art of record. This feature is not disclosed or suggested by the art of record, and it provides further isolation of the semiconductor substrate immediately beneath each insulator island, so that the active area under each insulator island is further isolated. Furthermore, these claims also recite a selective removal to form an upper surface for each isolation trench and spacers, where the selective removal is performed in the absence of masking of the conformal layer over the isolation trenches. These features are not disclosed or suggested by the '072 patent, and Poon does not provide any basis that would overcome the limitations and differences established with respect to the disclosure in the '072 patent. Furthermore, even if the '072 patent were combined with Poon, the combination would not disclose or suggest the method recited in these claims. Accordingly, it may not be asserted that the teachings provided by the '072 patent and/or Poon are sufficient for one of ordinary skill in the art to make the substitutions, combinations or other modifications that are necessary to arrive to the claimed methods.

Consequently, Applicants respectfully submit that the '072 patent and/or Poon do not support a *prima facie* case of obviousness regarding the present claims. Applicants respectfully request the reconsideration and withdrawal of this rejection.

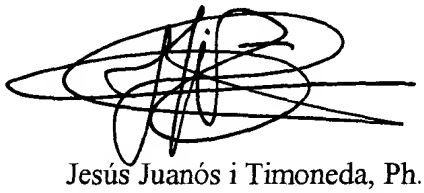
3. CONCLUSIONS

In view of the above, Applicants respectfully maintain that the present application is in condition for allowance. Reconsideration of the rejections is requested. Allowance of the pending claims at an early date is solicited.

In the event that the Examiner finds any remaining impediment to a prompt allowance of this application which could be clarified by a telephonic interview, or which is susceptible to being overcome by means of an Examiner's Amendment, the Examiner is respectfully requested to initiate the same with the undersigned attorney.

Dated this 13th day of August 2001.

Respectfully submitted,



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Marked up Version of the Pending Claims Under 37 C.F.R. § 1.121(c)(1)(ii):

Applicant submits the following marked up version only for claims being changed by the current amendment, wherein the markings, if any, are shown by brackets (for deleted matter) and/or underlining (for added matter).

1. (Once Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon said oxide layer;

selectively removing said first dielectric layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer over said oxide layer and said first dielectric layer;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas, and wherein each isolation trench has a top edge;

rounding the top edge of each of said isolation trenches;

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers; and

planarizing the conformal layer and each said spacer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein said planarizing is performed in the absence of masking the conformal layer over the isolation trench;

wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches.

7. (Once Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a first dielectric layer upon said oxide layer;

selectively removing said first dielectric layer to expose said oxide layer at a plurality of areas;

forming a second dielectric layer over said oxide layer and said first dielectric layer;

selectively removing said second dielectric layer to form a plurality of spacers from said second dielectric layer, wherein each said spacer is situated upon said oxide layer, is in contact with said first dielectric layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas, and wherein each isolation trench has an edge;

rounding the top edge of each of said isolation trenches;

filling each said isolation trench with a conformal layer, said conformal layer extending above said oxide layer in contact with a corresponding pair of said spacers;

planarizing with a single etch recipe the conformal layer to form therefrom an upper surface for each said isolation trench that is co-planar to the other said upper surfaces, wherein:

material that is electrically insulative extends continuously between and within said plurality of isolation trenches;

said conformal layer and said spacers form said upper surface for each said isolation trench, each said upper surface being formed from said conformal layer and said spacer and being situated above said pad oxide layer; and

said first dielectric layer is in contact with at least a pair of said spacers and said pad oxide layer.

14. (Twice Amended) A method of forming a microelectronic structure, the method comprising:

forming an oxide layer upon a semiconductor substrate;

forming a silicon nitride layer upon said oxide layer;

selectively removing said silicon nitride layer to expose said oxide layer at a plurality of areas;

forming a first silicon dioxide layer over said oxide layer and over said silicon nitride layer;

selectively removing said first silicon dioxide layer to form a plurality of spacers from said first silicon dioxide layer, wherein each said spacer is situated upon said oxide layer, is contact with said silicon nitride layer, and is adjacent to an area of said plurality of areas;

forming a plurality of isolation trenches extending below said oxide layer into and terminating within said semiconductor substrate, wherein each said isolation trench is adjacent to and below a pair of said spacers and is situated at a corresponding area of said plurality of areas, and wherein each isolation trench has a top edge;

forming a corresponding electrically active region below the termination of said each said isolation trench within said semiconductor substrate;

forming a liner upon a sidewall of each said isolation trench, said liner extending from an interface thereof with said oxide layer to the termination of said isolation trench within said semiconductor substrate;

rounding the top edge of each of said isolation trenches;

filling each said isolation trench with a conformal second silicon dioxide layer, said conformal second silicon dioxide layer within each said isolation trench extending above said oxide layer in contact with the corresponding pair of said spacers; and

selectively removing said conformal second silicon dioxide layer and said spacers to form an upper surface for each said isolation trench that is co-planar to the other said upper surfaces and being situated above said pad oxide layer, wherein material that is electrically insulative extends continuously between and within said plurality of isolation trenches, and wherein said selectively removing is performed in the absence of masking the conformal second silicon dioxide layer over each said isolation trench.

35. (Thrice Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon said oxide layer;

forming a first layer upon said polysilicon layer;

forming a plurality of isolation trenches having electrically insulative material extending continuously between and within said plurality of isolation trenches, each said isolation trench:

having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer[, wherein said spacer and said isolation trench are formed with a single etch recipe];

extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said spacer;

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer; [and]

<u>having a top edge and said top edge being rounded; and</u>

having a planar upper surface formed from said second layer and said spacer and being situated above said oxide layer; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches.

38. (Thrice Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon said oxide layer;

forming a plurality of isolation trenches having electrically insulative material extending continuously between and within said plurality of isolation trenches, each said isolation trench:

having a spacer composed of a dielectric material upon said oxide layer in contact with said first layer[, wherein said spacer and said isolation trench are formed with a single etch recipe];

extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said spacer;

having a second layer filling said isolation trench and extending above said oxide layer in contact with said spacer; [and]

<u>having a top edge and said top edge being rounded; and</u>

having a planar upper surface formed from said second layer and said spacer and being situated above said oxide layer; and

wherein the microelectronic structure is defined at least in part by the plurality of spacers, the second layer, and the plurality of isolation trenches.

41. (Thrice Amended) A method of forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface;

forming first and second isolation trenches each:

extending into and being defined by the semiconductor substrate;

having an opening thereto at the top surface of the semiconductor substrate;

having a top edge and said top edge being rounded; and

extending below and being centered between a pair of spacers situated above the top surface of the semiconductor substrate[, wherein said spacers and said isolation trenches are formed with a single etch recipe];

and wherein:

an electrically insulative material extends continuously between and within the first and second isolation trenches; and

a planar surface begins at the first isolation trench and extends continuously to the second isolation trench; and

wherein the microelectronic structure is defined at least in part by the pair of spacers, the electrically insulative material, and the first and second isolation trenches.

42. (Thrice Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a polysilicon layer upon said oxide layer;

forming a first layer upon said polysilicon layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

a first isolation trench extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer, wherein said first spacer is situated on a side of said first isolation trench, and wherein said first isolation trench has a top edge that is rounded;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer, said second spacer being situated on a side of said first isolation trench opposite the side of said first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer;

a first isolation trench extending below said oxide layer into and

terminating within said semiconductor substrate adjacent to and below said first spacer of said second isolation structure, wherein said first spacer of said second isolation structure is situated on a side of said first isolation trench, and wherein said first isolation trench in said second isolation structure has a top edge that is curved;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer and said polysilicon layer, said second spacer of said second isolation structure being situated on a side of said first isolation trench opposite the side of said first spacer of said second isolation structure;

forming an active area located within said semiconductor substrate between said first and second isolation structures;

forming a conformal second layer, composed of an electrically insulative material, filling said first and second isolation trenches and extending continuously therebetween and above said oxide layer in contact with said first and second spacers of said respective first and second isolation structures; and

forming with a single etch recipe a planar upper surface from said conformal second layer and said first and second spacers of said respective first and second isolation structures, and being situated above said oxide layer; and

wherein the microelectronic structure is defined at least in part by the active area, the second layer, and the first and second isolation trenches.

43. (Thrice Amended) A method for forming a microelectronic structure, the method comprising:

providing a semiconductor substrate having a top surface with an oxide layer thereon;

forming a first layer upon said oxide layer;

forming a first isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

a first isolation trench extending from an opening thereto at the top surface of said semiconductor substrate and below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer, wherein said first spacer is situated on a side of said first isolation trench, and wherein said first isolation trench has a top edge that is rounded;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer, said second spacer being situated on a side of said first isolation trench opposite the side of said first spacer;

forming a second isolation structure including:

a first spacer composed of a dielectric material upon said oxide layer in contact with said first layer;

a first isolation trench extending below said oxide layer into and terminating within said semiconductor substrate adjacent to and below said first spacer of said second isolation structure, wherein said first spacer

of said second isolation structure is situated on a side of said first isolation trench, and wherein said first isolation trench in said second isolation structure has a top edge that is rounded;

a second spacer composed of a dielectric material upon said oxide layer in contact with said first layer, said second spacer of said second isolation structure being situated on a side of said first isolation trench opposite the side of said first spacer of said second isolation structure;

forming an active area located within said semiconductor substrate between said first and second isolation structures;

forming a conformal second layer, composed of an electrically insulative material, conformally filling said first and second isolation trenches and extending continuously therebetween and above said oxide layer in contact with said first and second spacers of said respective first and second isolation structures; and

planarizing the conformal second layer and said first and second spacers of said respective first and second isolation structures to form a planar upper surface from said conformal second layer and said first and second spacers of said respective first and second isolation structures, and being situated above said oxide layer, wherein said planarizing is performed in the absence of masking the conformal second layer over each of said isolation trenches, and wherein the microelectronic structure is defined at least in part by the active area, the conformal second layer, and the first and second isolation trenches.